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Description

BACKGROUND OF THE INVENTION

This invention relates to a neural network circuit for executing image recognition processing.

Much interest has recently been shown in a field of neutral network in data processing. The neural network is brought up from simulation of a neuron structure of a brain of a living thing. Many neural networks are accomplished by a conventional von Neumann sequential computer whose processing speed is extremely low. Therefore, the neural network is now tried to be structured by exclusive electric circuits. There are various kinds of neural network structured by exclusive electric circuits, such as a multi-layered neural network. FIG.8 shows the multi-layered neural network which has neurons having branch ability and integration ability and is provided with an input layer, an output layer and an intermediate layer of multiple layers interposed therebetween.

The multi-layered neural network shown in FIG.8 has three layers of: an input layer composed of two neuron elements 111, 112 to which input vectors i=1, i=2 are respectively inputted, an output layer composed of two neuron elements 330, 340 respectively regarding outputs o=1, o=2, and an intermediate layer composed of six neuron elements 121 - 124, 131, 132 formed in two layers. The intermediate layer is disposed between the input layer and the output layer. Between neuron elements in the respective layers, synapse groups 41 - 43 are disposed for setting coupling load therebetween. Each coupling load of synapses of the synapse groups 41 - 43 is changeable by learning.

A neural network agreeing to a recognition object is structured by learning each coupling load of synapses of the synapse groups 41 - 43, changing each coupling load sequentially, adequately. As a learning method of each coupling load of synapses of the synapse groups 41 - 43, a back propagation method (BP method) is generally known in the art, which is very time consuming for learning and additional learning and whose learning algorithm is unsuitable for constructing the hardware.

A neural network circuit shown in FIG.9 is proposed which is capable of high speed initial learning and additional learning and whose algorithm is suitable for constructing the hardware.

The neural network circuit in FIG.9 is a neutral network developing the network structure in FIG.8 into a tree-like branch structure, and is a three-layered neural network provided with an input layer, an intermediate layer and an output layer. The input layer is composed of neuron elements 11-11, 12-11 for only branch operation to which input vectors i=1, i=2 are respectively inputted. The intermediate layer is composed of 24 neuron elements 11-21 - 11-24, 11-31 - 11-38, 12-21 - 12-24, 12-31 - 12-38 for only branch operation which are formed in two layers, and has networks 13-1, 13-2 in tree-like branch structure in number of input vectors i=1, i=2 of the input layer (i.e., two). The output layer is composed of two output neuron elements (output units) 310, 320 for only integration operation, which respectively regard outputs o=1, o=2, and sums outputs from the upper 16 neuron elements 11-31 - 11-38, 12-31 - 12-38 of the intermediate layer. Between the intermediate layer and the output layer a synapse group 4 is disposed for setting respective coupling loads between the neuron elements. The coupling loads of each synapse of the synapse group 4 are changeable by learning. In FIG.9, paths through 12-11 - 12-22 - 12-34 - 310 corresponds to paths through 112 - 122 - 132 - 330 in FIG.8. Wherein, each coupling load of synapse between the neuron elements 11-11 - 11-38 and each coupling load of synapse between the neuron elements 12-11 - 12-38 are not learned and are set necessarily according to a value of the input vector inputted into the respective neuron elements 11-11, 12-11 of the input layer.

As an example of network system which depends on only the value of the input vector and sets necessarily, without learning, the coupling load of synapse in three-like branch structure, such as shown in FIG.9, there is a network system called quantizer neuron which is disclosed in "Character Recognition System Using Network Comprising Layers By Function", Preliminary Material for Image Electronic Communication Society's National Conference 1990, pages 77 - 80 and "Multi-Functional Layered Network using Quantizer Neurons", Computer World '90, November. In this kind of network structure, the coupling loads of synapses of a final layer is changed independent form other synapses, which leads to high speed initial learning and additional learning and makes the learning algorithm suitable for constructing the hardware.

In the recognition method in the network system shown in FIG.9, output values of the two neuron elements 310, 320 for only integration operation which are provided at an output layer are judged as to which is the largest and the address of the neuron element whose output value is the largest is made a recognition result. In the integration method in the neuron elements 310, 320 of the final layer for integrating outputs of the neuron elements 11-31 - 11-38, 12-31 - 12-38 of the intermediate layer, the respective output values of the intermediate layer and the respective coupling loads set in the synapse group 4 are multiplied and summed for integration.

The integration method in neuron elements are explained, with reference to FIG.10.

In FIG.10, the output neuron elements 310, 320 and the synapse group 4 are identical with those in FIG.9. References f1 and f2 denote intermediate output values of the neuron elements 11-31, 11-32 in FIG.9 respectively. In accordance with the above-mentioned references, the neuron elements 11-31 - 12-38 are branch points of an input signal, so that an output value from the neuron element 11-31 to the output neuron element 310 and an output value

from the neuron element 11-31 to the output neuron element 320 are equal to each other and are indicated by f1. Respective coupling load calculations of synapses to the output neuron elements are executed by respective coupling calculation executing parts 4-11 - 4-22. The coupling load calculation executing part 4-11 is composed of a multiplier 112 and a coupling load coefficient W11 which is multiplied with the output value fl corresponding to the intermediate layer to output a multiplied result. The coupling load calculation executing parts 4-12 - 4-22 have the same function as the coupling load calculation executing part 4-11, and have a different coupling load coefficient from one another. The integration calculations in the output neuron elements 310, 320 are expressed in following respective equations. The thus integrated output values of the neuron elements 310, 320 are judged as to which is the largest, and an address of the neuron element whose output value is the largest is made a recognition result.

$$\text{output of output neuron element 310} = W11 \times f1 + W12 \times f2 + \ldots$$

$$\text{output of output neuron element 320} = W21 \times f1 + W22 \times f2 + \ldots$$

The learning algorithm in network system shown in FIG.9 uses the learning rule of Hebb, in which if the recognition result is false, the coupling load of the synapse group 4 to an output neuron element to be true is fortified until the value of the output neuron element to be true is the largest output value by a supervisor input in FIG.9. As to the fortifying method, the coupling load coefficient is added according to the output value of the neuron elements 11-31 - 11-38, 12-31 - 12-38.

The fortifying method of coupling load of the synapse is explained, with reference to FIG.11.

FIG.11 shows the coupling load W11 of FIG.10 in enlarged scale. The intermediate layer output f1 is added to the present coupling load W11 according to a learning signal. The change in coupling load by learning is expressed as follows:

$$W11 = W11 + f1$$

In the multi-layered neural network structure which has the intermediate layer of tree-like branch structure, executes integration of synapses by output neuron elements of the final layer and executes learning by changing the coupling loads of the synapses of the final layer, the coupling load change is executed independent from the other synapses, which leads to high speed initial learning and additional learning and makes the learning algorithm suitable for constructing the hardware.

Recognition accuracy in the above multi-layered neural network of tree-like brunch structure is, however, low in case where a new unlearned data is recognized after an initial learning. The inventors have studied the reasons and consider the following is one of the reasons: In case where some kinds of input data are all identified by learning in the above neural network and variance of one kind of input data is small, a coupling load of the synapse group to the output neuron elements for recognizing a data similar to the input data is inflated at learning of the similar data so as to clarify a difference between the similar data and the one-kind input data, with a result that the similar data is mis-recognized as an output result of output neuron element having as an input the inflated coupling load at next recognition of an unlearned data different from the similar data under such a condition since the inflated coupling load is extremely large compared with the other coupling loads of the unlearned data when the synapse group of the inflated coupling load is included in the synapse group to the output neuron element for the unlearned data recognition.

At the initial learning, the coupling load of synapse to the output neuron element is gradually increased according to the number of times at learning, which requires bit accuracy (bit word length) of coupling load and increases hardware in size which is required for coupling load memory. The above-mentioned references disclose that the coupling load memory of about 16 bits is required for 13-font learning of 62 kinds of character data according to a data group to be recognized. This means a large-sized hardware required for the coupling load memory.

SUMMARY OF THE INVENTION

The object of the invention is providing a neural network circuit capable of solving the problems in the neural network of tree-like branch structure, of improving a recognition accuracy for unlearned data and of reducing the amount of hardware required for coupling load memory.

To attain the above object, in the multilayered neural network of the present invention, connection of the synapses to the output neuron elements is controlled by learning, thus differing from the conventional neural network circuits wherein the coupling load of synapses to the output neuron elements is calculated by means of weights.

A multi-layered neural network circuit according to the present invention is provided as set out in claims 1 and 5.

In a further embodiment of the neural network circuit, each output of the intermediate layer has two kinds of values of "HIGH" and "LOW", and the respective output units count the number of "HIGH"s among the outputs of the intermediate layer connected by the respective connection control circuits.

According to the neural network circuit with the above construction, the number of learning times of synapses to the output neuron elements is memorized in the learning-time memory, and only paths between the outputs whose numbers of learning times (number of times that non-zero values are outputted or number of times that each of the outputs exceeds the set value in each output of the neuron elements within the intermediate layer of network in tree-like branch structure) exceed the set threshold among outputs of the neuron elements within the intermediate layer and the respective output neuron elements are connected by the connection control circuit only when the number of learning times exceeds the set threshold. As a result, each output neuron element executes summation of all outputs of the neuron elements within the intermediated layer to recognize the input data. The input data recognition depends on the path connection between the outputs whose numbers of learning times exceed the set threshold among the outputs of the neuron elements within the intermediate layer and the respective output neuron elements. Since no weight are used in the connected paths, the local inflation in coupling load of synapse as the conventional one does not occur, thus enhancing the recognition accuracy for unlearned data.

By clipping the number of learning times in the learning-time memory to the upper limit value, the hardware size required for memorizing the number of learning times is reduced.

Many paths among paths between outputs of neuron elements within the intermediate layer and the output units are connected unnecessarily owing to excessive learning. However, the unnecessary paths are disconnected so as to connect only the necessary paths by subtracting the set value from each number of learning times in all learning-time memories or by increasing the threshold of the threshold processing circuit by the set value. Thus, noise component of data to be recognized at excessive learning is reduced, while further enhancing the recognition accuracy for unlearned data.

Moreover, in one embodiment of the neural network circuit of the present invention, instead of learning-time memory, the flag memory is provided for memorizing the presence of learning history of synapses to the output neuron elements, which further reduces the amount of hardware.

Instead of summation of output values of the intermediate layer being achieved by the respective output neural elements of the output layer, the number of times that outputs of non-zero value among outputs of neuron elements within the intermediate layer are outputted are counted, which further reduces the hardware amount of the integration circuit including the output layer.

Other objects and features of the neural network circuit of the present invention will appear more fully from the following description with accompanying drawings.

BRIEF DESCRIPTION OF THE ACCOMPANYING DRAWINGS

Accompanying drawings show preferable embodiments of the present invention, in which:

FIG.1 is a diagram showing a construction of a neural network circuit in a first embodiment;
FIG.2 is a diagram of a learning calculation circuit of a learning-time memory;
FIG.3 is a diagram of a learing calculation circuit showing a first modified example of learning-time memory;
FIG.4 is a diagram of a learning calculation circuit showing a second modified example of learning-time memory;
FIG.5 is a diagram showing a construction of a neural network circuit in a second embodiment;
FIG.6 is a diagram showing a construction of a neural network circuit in a third embodiment;
FIG.7 is a diagram showing a construction of a neural network circuit in a fourth embodiment;
FIG.8 is a diagram showing a construction of a conventional multi-layered network circuit;
FIG.9 is a diagram showing a construction of a conventional multi-layered network circuit in tree-like branch structure;
FIG.10 is a diagram for explaining an integration method of integral neuron elements in the conventional multi-layered neural network circuit in tree-like branch structure; and
FIG.11 is a diagram of a conventional coupling load calculation circuit of a coupling load memory.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Description is made below about preferred embodiments of the present invention, with reference to accompanying drawings.

FIG.1 shows a construction of a neural network circuit, and corresponds to the conventional example in FIG.10. As far as is possible the same reference numerals have been used as in FIG.10.

In FIG.1, reference numerals 310 and 320 are output neuron elements of a final layer for integrating intermediate layer outputs of neuron elements 11-31 - 11-38, 12-31 - 12-38 in FIG.9. References f1 and f2 are, as mentioned in the conventional example, intermediate layer output values of neuron elements 11-31 and 11-32 in FIG.9 respectively. In accordance with the above mentioned references, the neuron elements 11-31 - 12-38 are branch points of an input signal, so that an output value from the neuron element 11-31 to the output neuron element 310 and an output value from the neuron element 11-31 to the output neuron element 320 are equal to each other and are indicated by fl. The calculation of connection of synapses to the output neuron elements is executed by connection calculation executing parts 4-11 - 4-22.

The connection calculation executing part 4-11 is composed of a learning-time memory 113, a threshold processing circuit 114 for threshold-processing the learning-time memory 113, namely for comparing the number of learning times stored in the corresponding learning-time memory 113 with a set threshold and for outputting a first set value when the number of learning times of the corresponding learning-time memory is equal to or more than the threshold and outputting a second set value when the number of times at learning of the corresponding learning-time memory is less than the threshold, and a connection control circuit 115 controlled by two kinds of control signals from the threshold processing circuit 114. The connection control circuit 115 controls connection synapses between the neuron elements within the intermediate layer and the output neuron elements. The connection calculation executing parts 4-12 - 4-22 have the same function as of the connection calculation executing part 4-11, and have a different number of times at learning from one another. If the threshold of the threshold processing circuit 114 is 1, the intermediate layer output f1 is outputted when the learning-time value R11 (the number of times at learning) of the learning-time memory 113 in the connection calculation executing part 4-11 is 1 or more and 0 is outputted without connection of the intermediate layer output f1 when the learning-time value R11 of the learning-time memory 113 is 0. In the output neuron elements 310, 320, only the intermediate layer outputs of connected synapses are added for integration among the intermediate layer outputs.

The thus integrated output values of the output neuron elements 310, 320 are judged as to which is the largest so as to make an address of the output neuron element whose output value is the largest a recognition result.

Learning algorithm in the network system shown in FIG.1 is discussed next.

First, all learning-time memories of synapses continuing to the output neuron elements are set 0. Then, an initial learning is executed only one time to all data to be initial-learned. The learning method is as follows: the values in all learning-time memories of synapses whose intermediate layer outputs are not 0 are incremented by a supervisor input in FIG.1 through connection synapses connected to the output neuron elements corresponding to the input data. It may be possible to increment the values in the learning-time memories of synapses whose intermediate layer outputs are equal to or more than a threshold.

FIG.2 shows an example of an updater of the learning-time memory 113 in FIG.1 in enlarged scale. The present learning-time value R11 is incremented by 1 according to a learning signal. Change in number of learning times by learning is expressed by the following equation:

$$R11 = R11 + 1$$

As described above, in this embodiment, the number of learning times of a synapse connected to the output neuron elements is memorized, and only the outputs of neuron elements within the intermediate layer from synapses whose numbers of learning times exceed the threshold are summed. Thus, the local inflation in coupling load of synapse due to small variance of one kind of input data in addition to similar data is prevented and the recognition accuracy for unlearned data is enhanced.

FIG.3 shows a modified example of a learning calculation circuit of the learning-time memory 113. As shown in FIG.3, an upper limiter 113 as upper limit clipping means is provided on the input side of the learning-time memory 113. This reduces a memory capacity of the learning-time memory 113. Different from the conventional construction wherein the coupling load of the synapses to the output neuron elements is calculated by means of weights, in the present invention, the connection synapses to the output neuron elements is calculated according to the number of learning times.

When a limit value (upper limit of the number of learning times) of the upper limiter 113a shown in FIG.3 is set to 3, only two bits are required for memorizing the number of learning times, which is one eighth of 16-bit coupling load memory in the conventional one. Further, the recognition accuracy is increased to about 86% (63% in the conventional one) in a recognition test for unlearned data after the initial learning according to the present invention with the neural network construction in the above mentioned references. In the recognition test, 62 kinds of 13-font character data are learned at the initial learning and the recognition accuracy for 62 kinds of 10-font unlearned character data is calculated.

According to the present invention, the recognition accuracy for unlearned data is excellent even with less memory capacity required for learning.

According to the neural network circuit with the above construction, one-time learning to one input data makes the value of the corresponding output neuron element the largest for the same input data without exception, thus enabling the initial learning without recognition result with no conditions. Accordingly, the convergence time at the initial learning in the neural network construction in the present invention is about one sixtieth to one thousandth of that in the conventional one.

While the learning-time memory 113 in FIG.3 has an excellent feature, a problem arises that the recognition accuracy for unlearned data is lowered owing to excessive learning. Because, the synapses to the output neuron elements are unnecessarily connected, receiving many noise components by excessive learning. However, the lowering of the recognition accuracy for unlearned data due to excessive learning is prevented by regarding the synapses which are not so learned in past learning as noise components and ignoring the learning history.

FIG.4 shows an example of an updater of the learning-time memory which solves the problem which is another modification of the learning-time memory 113 in FIG.1. The learning-time memory in FIG.4 includes a selector 113b as a learning-time updater having a function of decrementing by one the present learning-time value R11 according to a learning signal, in addition to the incrementing function shown in FIG.2. The selector 113b receives a control signal for subtraction. When the control signal for subtraction is inputted, the selector 113b outputs -1 to an adder 113c, halting the incrementing function, to decrement by 1 the present learning-time value R11. Further, the learning-time memory includes a lower limiter 113d as lower limit clipping means which has a function of limiting a value less than 0 to 0.

When the recognition accuracy for unlearned data is lowered due to excessive learning, 1 is subtracted from all learning-time values stored in the learning-time memories of the synapses to the output neuron elements according to the control signal for subtraction. Wherein, the learning-time value R11 less than 0 is limited to 0 by the lower limiter 113d. With the above function added, the lowering of the recognition accuracy for unlearned data due to excessive learning is prevented.

As to means for preventing the lowering of the recognition accuracy for unlearned data due to excessive learning, the same effect can be obtained by adding 1 to the threshold of the threshold processing circuit 114 in FIG.1, besides the method showing in FIG.4.

The updater of the learning-time memory subtracts 1 in this embodiment, but may execute division if it has the function of decreasing the number of times at learning.

FIG.5 shows a construction of a neural network circuit in a second embodiment, and corresponds to FIG.10 of the conventional example, so the same reference numerals as in FIG.10 have been used for the same elements in FIG.5.

In FIG.5, reference numerals 310 and 320 are output neuron elements of the final layer for integrating intermediate layer outputs of the neuron elements 11-31 - 11-38, 12-31 - 12-38. References f1 and f2 are, as mentioned in the conventional example, the intermediate layer output values of the neuron elements 11-31 and 11-32 in FIG.9 respectively. In accordance with the above mentioned references, the neuron elements 11-31 - 12-38 are branch points of an input signal, so that an output value from the neuron element 11-31 to the output neuron element 310 and an output value from the neuron element 11-31 to the output neuron element 320 are equal to each other and are indicated by f1. The calculation of connection synapses to the respective output neuron elements is executed by the connection calculation executing parts 4-11 - 4-22.

The connection calculation executing part 4-11 is composed of a flag memory 116 and a connection control circuit 115 to be controlled by the flag memory 116 for controlling connection synapses between neuron elements within the intermediate layer and the output neuron elements. The connection calculation executing parts 4-12 - 4-22 have the same function as that of the connection calculation executing part 4-11, and have a different flag value from one another. The intermediate layer output f1 is outputted when a value Q11 of the flag memory 116 in the connection calculation executing part 4-11 is 1 and 0 is outputted without connection of the intermediate layer output f1 when the value Q11 of flag memory 116 is 0. In the output neuron elements 310, 320, only the intermediate layer outputs of connected synapses are added for integration among the intermediate layer outputs. The thus integrated output values of the neuron elements 310, 320 are judged as to which is the largest so as to make an address of the output neuron element whose output value is the largest a recognition result.

The learning algorithm in the network system shown in FIG.5 is discussed next.

First, all flag memories of synapses connected to the output neuron elements are set to 0. Suppose that the outputs of the neuron elements within intermediate layer output are not connected to the output neuron elements when the flag memory is 0 and are connected thereto when the flag memory is 1. Then, at the initial learning, learning is executed only one time to all of the data to be initial-learned. The learning method is that: 1 is set by a supervisor input in FIG. 5 to all values in the flag memories of synapses whose intermediate layer outputs are not 0 among the synapses connected to the output neuron elements corresponding to the input data. Setting to 1 may be conducted to the flag memories whose intermediate layer output is equal to or more than a set threshold, instead of non-zero intermediate layer value.

As described above, in this embodiment, the flag memory requires only one-bit memory capacity for one synapse, which means further reduction of memory capacity than in the first embodiment. Since the threshold processing circuit

for the learning-time memory is unnecessary, the size of the hardware is expected to reduce. As to the recognition accuracy for unlearned data, the equivalent performance is obtained as in the neural network circuit in the first embodiment.

According to the neural network circuit of the present invention, the recognition accuracy for unlearned data is excellent even with less memory capacity of the flag memory which is required for learning.

Further, in the neural network circuit with the above construction, one-time learning to one input data makes the value of the corresponding output neuron element the largest for the same input data without exception, which enables the initial learning without recognition result with no conditions. Accordingly, the convergence time at the initial learning in the neural network construction of the present invention is about one sixtieth to one thousandth of that in the conventional one.

In the neural network circuit in this embodiment, the recognition accuracy for unlearned data is lowered because of excessive learning. However, such the low recognition accuracy can be ignored in cases of initial learning not to be excessive learning, of learning of data with less noise component or of use of the flag memory in ROM construction as a recognition device.

FIG.6 shows a neural network circuit according to a third embodiment, and corresponds to FIG.5 of the conventional example, so the same reference numerals as in FIG.5 have been used for the same elements in FIG.6.

In FIG.6, reference numerals 310 and 320 are the output neuron elements of the final layer for integrating intermediate layer outputs of the neuron elements 11-31 - 11-38, 12-31 - 12-38. References f1 and f2 are, as described in the conventional example, the intermediate layer output values of the neuron elements 11-31 and 11-32 in FIG.9 respectively. In accordance with the above mentioned references, the neuron elements 11-31 - 12-38 are the branch points of an input signal, so that an the output value from the neuron element 11-31 to the output neuron element 310 and an output value from the neuron element 11-31 to the output neuron element 320 are equal to each other and are indicated by f1. Wherein, in FIG.6, there are two kinds, i.e. 1 and 0, of intermediate layer output values f1, f2. The calculation of the connection synapses to the respective output neuron elements is executed by the connection calculation executing parts 4-11 - 4-22.

The connection calculation executing part 4-11 is composed of the flag memory 116 and a connection control circuit 117 to be controlled by the flag memory 116 for controlling the connection of synapse between the intermediate layer and the output neuron elements. The connection calculation executing parts 4-12 - 4-22 have the same function as the connection calculation executing part 4-11, and have a different flag value from one another. Since the connection control circuit 117 receives two kinds of input values from the intermediate layer, a logical product circuit, instead of the selector shown in FIG.5, can serve as the connection control circuit 117. In the output neuron elements 310, 320, the number of ones of outputs of neuron elements within the intermediate layer of connected synapses to neuron elements of the output layer are counted for integration.

The thus integrated output values of the output neuron elements 310, 320 are judged as to which is the largest so as to make an address of the output neuron element whose output value is the largest a recognition result.

The learning algorithm in the network system shown in FIG.6 is discussed next.

First, all flag memories of synapses continuing to the output neuron elements are set to 0. Suppose that outputs of neuron elements within the intermediate layer are not connected to the output neuron elements when the flag memory is 0 and is connected thereto when the flag memory is 1. Then, at the initial learning, learning is executed only one time to all of the data to be initial-learned. The learning method is that: 1 is set by a supervisor input in FIG.6 to all values in the flag memories of synapses whose intermediate layer outputs are 1 among the synapses connected to the output neuron elements corresponding to the input data.

By employing the neural network circuit of the invention in the second embodiment and in this embodiment, the connection control circuit 117 of the synapse to the output neuron elements is simplified and the integration processing which is executed in the output neuron elements 310, 320 is executed by counting the number of inputted values of 1, thus reducing the hardware size, compared with the circuit shown in FIG.5.

Upon a test of recognition accuracy for unlearned data, about 2 - 3% lowering of recognition accuracy is caused compared with the circuits in first and second embodiments. However, the recognition accuracy is much higher than that in the conventional learning method, which means applicable into practice depending on a kind of data to be recognized.

FIG.7 shows a neural network circuit according to a fourth embodiment of the present invention and corresponds to FIG.1, so the same reference numerals as in FIG.1 have been used for the same elements in FIG.7.

In FIG.7, reference numerals 310 and 320 are output neuron elements of the final layer for integrating the intermediate layer outputs of the neuron elements 11-31 - 11-38, 12-31 - 12-38 shown in FIG.9. References f1 and f2 are, as mentioned in the conventional example, the intermediate layer output values of the neuron elements 11-31 and 11-32 in FIG.9 respectively. In accordance with the above mentioned references, the neuron elements 11-31 - 12-38 are the branch points of an input signal, so that an output value from the neuron element 11-32 to the output neuron element 310 and an output value from the neuron element 11-32 to the output neuron element 320 are equal to each

other and are indicated by f1. Wherein, in FIG.7, the intermediate layer output values f1, f2 have two kinds of outputs, i.e. 1 and 0. The calculation of connection of the synapse to the output neuron elements is executed by the connection calculation executing parts 4-11 - 4-22.

The connection calculation executing part 4-11 is composed of the learning-time memory 113, the threshold processing part 114 for threshold-processing the learning-time memory 113 and the connection control circuit 117 to be controlled by the control signal of two kinds of values by the threshold processing circuit 114 for controlling the connection synapses between the neuron elements within intermediate layer and the output neuron elements. The connection calculation executing parts 4-12 - 4-22 have the same function as that of the connection calculation executing part 4-11, and have a different learning-time value from one another. Since the connection control circuit 117 receives two kinds of values from the intermediate layer, a logical product circuit, instead of the selector shown in FIG. 1, can serve as the connection control circuit 117. In the output neuron elements 310, 320, the number of outputs having a value of 1 of the neuron elements within the intermediate layer of the connection synapses is counted for integration.

The thus integrated output values of the neuron elements 310, 320 are judged as to which is the largest so as to make an address of the output neuron element whose output value is the largest a recognition result.

According to the circuit shown in FIG.6, the connection control circuit 117 of the synapse to the output neuron elements is simplified and the integration processing executed in the output neuron elements 310, 320 is executed by counting the number of input values of 1, thus reducing the hardware size, compared with the circuit shown in FIG.1.

Similar to the circuit shown in FIG.6, the recognition result for the unlearned data is about 2 - 3% lower than that in the first embodiment shown in FIG.1 and that in the second embodiment shown in FIG.5. However, the recognition accuracy thereof is much higher than that in the conventional learning method and the circuit is applicable into practice depending on a kind of data to be recognized. The circuit shown in FIG.7 can prevent the lowering of the recognition accuracy for unlearned data due to excessive learning, as well as the circuit in FIG.1.

In the above embodiments, each connection calculation executing part 4-11 - 4-22 requires a memory for memorizing a different learning value. However, the processing in each connection calculation executing part and the integration processing in the output neuron elements can be executed by using one or plural processing devices, sequentially exchanging the learning memories. Moreover, as described in this embodiment, the connection calculation executing parts may be provided at all synapses to the respective output neuron elements to execute parallel processing.

The two output neuron elements are discussed for the sake of simplicity, but the neural network circuit of the present invention is not limited to this example, and may have another number of outputs.

Claims

1. A multi-layered neural network circuit provided with an input layer (11-11 - 12-11) to which one or plural input vectors are inputted, an intermediate layer (11-31 - 11-38,12-31 - 12-38) having neuron elements connected in tree-like structure whose outputs are necessarily determined by values of the input vectors and whose number corresponds to the number of the input vectors of the input layer, and an output layer having one or plural output neuron elements (310,320) for integrating all output values of neuron elements within the intermediate layer, the calculation of connection of synapses to the output neuron elements (310, 320) being executed by connection calculating executing parts (4-11 - 4-22), said connection calculating executing parts comprising:

   learning-time memorie (113), respectively provided so as to correspond to respective paths which connect respective outputs of neurons located within the intermediate layer with the respective output neuron elements, for respectively memorizing the number of learning times or number of times that an output value of the neuron elements within the intermediate layer is outputted to a corresponding path to the output neuron elements is equal to or more than a set value;
   threshold processing circuits (114), respectively provided so as to compare the number of learning times stored at said learning-time memories with a set threshold value, for outputting a first set value when a number of learning times which is stored in the corresponding learning-time memory is equal to or more than said set threshold and outputting a second set value when a number of times at learning which is stored in the corresponding learning-time memory is less than said set threshold, and
   connection control circuits (115) for respectively connecting the respective paths between the respective outputs of the neuron elements within the intermediate layer and the respective output neuron elements when an output of the corresponding threshold processing circuits (114) is said first set value and disconnecting the respective paths therebetween when an output of the corresponding threshold processing circuits (114) is said second set value,
   wherein the respective output units sum the output values of the intermediate layer connected by the respective

connection control circuits.

2. The neural network circuit according to Claim 1, further comprising upper limit clipping means (113a) for respectively clipping the number of learning times stored in the respective learning-time memories to a set upper limit or threshold.

3. The neural network circuit according to Claim 1, further comprising:

learning-time updaters (113b) for respectively subtracting a set value from the number of learning times stored in the respective learning-time memories (113); and
lower limit clipping means (113d) for respectively clipping an subtracted result of the number of times at learning which is less than 0 to 0.

4. The neural network circuit according to Claim 1, wherein the threshold processing circuits have a function of changing a threshold to a set value.

5. A multi-layered neural network circuit provided with an input layer to which one or plural input vectors are inputted, an intermediate layer (4-11 - 4-12, 4-21 - 4-22) having neuron elements connected in tree-like structure whose outputs are necessarily determined by values of the input vectors and whose number corresponds to the number of the input vectors to the input layer, and an output layer having one or plural output neuron elements (310,320) units for integrating all output values of said neuron elements within the intermediate layer, comprising:

flag memories (116), respectively provided to respective paths connecting respective outputs of the intermediate layer and the respective output units, for respectively memorizing the learning times or times where output values of neuron elements within the intermediate layer are outputted to the corresponding path to said output neuron elements, when said outputs were equal to or more than a set value in the past, and for outputting a set value upon learning and outputting another set value in the absence of learning; and
connection control circuits (115) for respectively controlling connection and disconnection of the paths between the respective outputs of said neuron elements within the intermediate layer and respective output neuron elements according to an output of the respective flag memories (116),
wherein the respective output units sum the output values of said neuron elements within the intermediate layer connected by the respective connection control circuits.

6. The neural network circuit according to Claim 1 or 5, wherein each output of said neuron elements within the intermediate layer has two kinds of values of "HIGH" and "LOW", and the respective output neuron elements count the number of "HIGH"s among the outputs of said neurons within the intermediate layer connected by respective connection control circuits (115).

Patentansprüche

1. Vielschichtige neuronale Netzschaltung mit einer Eingabeschicht (11-11 - 12-11), in die ein oder mehrere Eingabevektoren eingegeben werden, einer Zwischenschicht (11-31 - 11-38, 12-31 - 12-38), die in einer baumartigen Struktur miteinander verbundene Neuronenelemente aufweist, deren Ausgaben notwendigerweise durch die Werte der Eingabevektoren bestimmt werden und deren Anzahl der Anzahl der Eingabevektoren der Eingabeschicht entspricht, und einer Ausgabeschicht mit einem oder mehreren Ausgabe-Neuronenelementen (310,320) zum Integrieren aller Ausgabewerte der Neuronenelemente in der Zwischenschicht, wobei die Berechnung der Verbindung der Synapsen zu den Ausgabe-Neuronenelementen (310,32=) durch Verbindungsberechnungs-Ausführteile (4-11 - 4-22) vorgenommen wird, wobei die Verbindungsberechnungs-Ausführteile umfassen:

Lernhäufigkeitsspeicher (113), die jeweils für entsprechende Pfade, die entsprechende Ausgaben der Neuronen in der Zwischenschicht mit entsprechenden Ausgabe-Neuronenelementen verbinden, vorgesehen sind und die Lernhäufigkeit oder die Häufigkeit speichern, mit der ein Ausgabewert, der von den Neuronenelementen in der Zwischenschicht zu einem entsprechenden Pfad zu den Ausgabe-Neuronenelementen ausgegeben wird, größer oder gleich einem gesetzten Wert ist,

Schwellwertverarbeitungsschaltungen (114), die jeweils vorgesehen sind, um die in den Lernhäufigkeitsspeichern gespeicherte Lernhäufigkeit mit einem gesetzten Schwellwert zu vergleichen, um einen ersten gesetzten

Wert auszugeben, wenn die in dem entsprechenden Lernhäufigkeitsspeichern gespeicherte Lernhäufigkeit größer oder gleich dem gesetzten Schwellwert ist, und um einen zweiten gesetzten Wert auszugeben, wenn die in dem entsprechenden Lernhäufigkeitsspeicher gespeicherte Lernhäufigkeit kleiner als der gesetzte Schwellwert ist, und

Verbindungssteuerschaltungen (115), um jeweils die entsprechenden Pfade zwischen den entsprechenden Ausgaben der Neuronenelemente in der Zwischenschicht und den entsprechenden Ausgabe-Neuronenelementen zu verbinden, wenn eine Ausgabe der entsprechenden Schwellwertverarbeitungsschaltungen (114) den ersten gesetzten Wert aufweist, und um die Pfade jeweils zu unterbrechen, wenn eine Ausgabe der entsprechenden Schwellwertverarbeitungsschaltungen (114) gleich dem gesetzten Wert ist,

wobei die entsprechenden Ausgabeeinheiten die Ausgabewerte der durch die entsprechenden Verbindungssteuerschaltungen verbundenen Zwischenschicht summieren.

2. Neuronale Netzschaltung nach Anspruch 1, die weiterhin eine Obergrenzen-Abschneideeinrichtung (113a) umfaßt, um jeweils die in den entsprechenden Lernhäufigkeitsspeichern gespeicherten Lernhäufigkeiten auf einen gesetzten Obergrenzwert abzuschneiden.

3. Neuronale Netzschaltung nach Anspruch 1, die weiterhin umfaßt:

Lernhäufigkeits-Aktualisierer (113b), um jeweils einen gesetzten Wert von der in den entsprechenden Lernhäufigkeitsspeichern (113) gespeicherten Lernhäufigkeit zu subtrahieren, und

eine Untergrenzen-Abschneideeinrichtung (113d), um ein Subtraktionsergebnis der Lernhäufigkeit, das kleiner ist als 0 auf 0 abzuschneiden.

4. Neuronale Netzschaltung nach Anspruch 1, wobei die Schwellwertschaltungen die Funktion haben, einen Schwellwert zu einem gesetzten Wert zu ändern.

5. Vielschichtige neuronale Netzschaltung, mit einer Eingabeschicht, in die ein oder mehrere Eingabevektoren eingegeben werden, einer Zwischenschicht (4-11 - 4-12, 4-21 - 4-22), die in einer baumartigen Struktur miteinander verbundene Neuronenelemente aufweist, deren Ausgaben notwendigerweise durch die Werte der Eingabevektoren bestimmt werden und deren Anzahl der Anzahl der Eingabevektoren der Eingabeschicht entspricht, und einer Ausgabeschicht mit einem oder mehreren Ausgabe-Neuronenelementen (310,320) zum Integrieren aller Ausgabewerte der Neuronenelemente in der Zwischenschicht, wobei die neuronale Netzschaltung umfaßt:

Flagspeicher (116), die jeweils für entsprechende Pfade vorgesehen sind, die entsprechende Ausgaben der Zwischenschicht und der entsprechenden Ausgabeeinheiten verbinden, um jeweils die Lernhäufigkeit oder die Häufigkeit zu speichern, mit der die Neuronenelemente in der Zwischenschicht zu dem entsprechenden Pfad zu den Ausgabe-Neuronenelementen ausgegeben werden und die Ausgaben größer oder gleich einem zuvor gesetzten Wert sind, und um einen gesetzten Wert auszugeben, wenn gelernt wurde, und um einen anderen gesetzten Wert auszugeben, wenn nicht gelernt wurde, und

Verbindungssteuerschaltungen (115), um jeweils die Verbindung und Unterbrechung der Pfade zwischen den entsprechenden Ausgaben der Neuronenelemente in der Zwischenschicht und den entsprechenden Ausgabe-Neuronenelementen in Übereinstimmung mit den entsprechenden Flagspeichern (116) zu steuern,

wobei die entsprechenden Ausgabeeinheiten die Ausgabewerte der Neuronenelemente in der durch die entsprechenden Verbindungssteuerschaltungen verbundenen Zwischenschicht summieren.

6. Neuronale Netzschaltung nach Anspruch 1 oder 5, wobei jede Ausgabe der Neuronenelemente in der Zwischenschicht zwei Arten von Werten "HIGH" oder "LOW" aufweist, wobei die entsprechenden Ausgabe-Neuronenelemente die Anzahl der "HIGH"s in den Ausgaben der Neuronenelementen in der durch die entsprechenden Steuerschaltungen (115) verbundenen Zwischenschicht zählt.

Revendications

1. Circuit de réseau neuronal multicouche muni d'une couche d'entrée (11-11 à 12-11) dans laquelle un ou plusieurs vecteurs d'entrée sont entrés, d'une couche intermédiaire (11-31 à 11-3B, 12-31 à 12-3B) ayant des éléments de neurone connectés en une structure du type arbre dont les sorties sont nécessairement déterminées par des valeurs des vecteurs d'entrée et dont le nombre correspond au nombre des vecteurs d'entrée de la couche d'entrée, et d'une couche de sortie ayant un ou plusieurs éléments de neurone de sortie (310, 320) pour intégration de toutes les valeurs de sortie des éléments de neurone à l'intérieur de la couche intermédiaire, le calcul de la connexion des synapses avec les éléments de neurone de sortie (310, 320) étant exécuté par des parties d'exécution de calcul de connexion (4-11 à 4-22), lesdites parties d'exécution de calcul de connexion comprenant :

   des mémoires de nombre de fois d'apprentissage (113) respectivement prévues de façon à correspondre aux trajets respectifs qui connectent les sorties respectives des neurones placées à l'intérieur de la couche intermédiaire avec les éléments de neurone de sortie respectifs pour mémoriser respectivement le nombre de fois d'apprentissage ou le nombre de fois où une valeur de sortie des éléments de neurone à l'intérieur de la couche intermédiaire qui est sortie sur un trajet correspondant vers les éléments de neurone de sortie, est égale ou supérieure à une valeur établie ;
   des circuits de traitement de seuil (114) respectivement prévus de façon à comparer le nombre de fois d'apprentissage mémorisé dans la mémoire de nombre de fois d'apprentissage à ladite valeur de seuil établie, pour sortir une première valeur établie lorsque le nombre de fois d'apprentissage qui est mémorisé dans la mémoire de nombre de fois d'apprentissage correspondante est égal ou supérieur audit seuil établi et pour sortir une seconde valeur établie lorsque le nombre de fois d'apprentissage qui est mémorisé dans la mémoire de nombre de fois d'apprentissage correspondante est inférieur audit seuil établi ; et
   des circuits de commande de connexion (115) pour connecter respectivement les trajets respectifs entre les sorties respectives des éléments de neurone à l'intérieur de la couche intermédiaire et les éléments de neurone de sortie respectifs lorsqu'une sortie des circuits de traitement de seuil correspondants (114) est ladite première valeur établie et déconnecter les trajets respectifs entre ceux-ci lorsqu'une sortie des circuits de traitement de seuil correspondants (114) est ladite seconde valeur établie,
   dans lequel les unités de sortie respectives somment les valeurs de sortie de la couche intermédiaire connectée par les circuits de commande de connexion respectifs.

2. Circuit de réseau neuronal selon la revendication 1, comprenant de plus un moyen de fixation de limite supérieure (113a) pour fixer respectivement le nombre de fois d'apprentissage mémorisé dans les mémoires de nombre de fois d'apprentissage respectives à une limite ou seuil supérieur établi.

3. Circuit de réseau neuronal selon la revendication 1, comprenant de plus :

   des circuits de mise à jour de nombre de fois d'apprentissage (113b) pour soustraire respectivement une valeur établie du nombre de fois d'apprentissage mémorisé dans les mémoires de nombre de fois d'apprentissage respectives (113) ; et
   un moyen de fixation de limite inférieure (113d) pour fixer respectivement un résultat soustrait du nombre de fois d'apprentissage qui est inférieur à 0 à 0.

4. Circuit de réseau neuronal selon la revendication 1, dans lequel les circuits de traitement de seuil ont pour fonction de changer un seuil à une valeur établie.

5. Circuit de réseau neuronal multicouche muni d'une couche d'entrée dans laquelle un ou plusieurs vecteurs d'entrée sont entrés, d'une couche intermédiaire (4-11 - 4-12, 4-21 - 4-22) ayant des éléments de neurone connectés en une structure de type arbre dont les sorties sont nécessairement déterminées par des valeurs des vecteurs d'entrée et dont le nombre correspond au nombre des vecteurs d'entrée dans la couche d'entrée, d'une couche de sortie ayant une ou plusieurs unités d'éléments de neurone (310, 320) pour intégrer toutes les valeurs de sortie desdits éléments de neurone à l'intérieur de la couche intermédiaire, comprenant :

   des mémoires d'indicateurs (116) respectivement prévues sur les trajets respectifs connectant les sorties respectives de la couche intermédiaire et les unités de sortie respectives, pour mémoriser respectivement les nombres de fois d'apprentissage ou les nombres de fois où des valeurs de sortie des éléments de neurone à l'intérieur de la couche intermédiaire sont sorties sur le trajet correspondant vers lesdits éléments de neurone de sortie, lorsque lesdites sorties étaient égales ou supérieures à une valeur établie dans le passé et pour

sortir une valeur établie sur apprentissage et pour sortir une autre valeur établie en l'absence d'apprentissage ; et

des circuits de commande de connexion (115) pour commander respectivement la connexion et la déconnexion des trajets entre les sorties respectives desdits éléments de neurone à l'intérieur de la couche intermédiaire et desdits éléments de neurone de sortie respectifs en conformité avec une sortie des mémoires d'indicateurs respectives (116),

dans lequel les unités de sortie respectives somment les valeurs de sortie desdits éléments de neurone à l'intérieur de la couche intermédiaire connectée par les circuits de commande de connexion respectifs.

6. Circuit de réseau neuronal selon la revendication 1 ou 5, dans lequel chaque sortie desdits éléments de neurone à l'intérieur d'une couche intermédiaire a deux types de valeurs "HAUTE" et "BASSE" et les éléments de neurone de sortie respectifs comptent le nombre de valeurs "HAUTES" parmi les sorties desditse neurones à l'intérieur de la couche intermédiaire connectés par les circuits de commande de connexion respectifs (115).

Fig.1

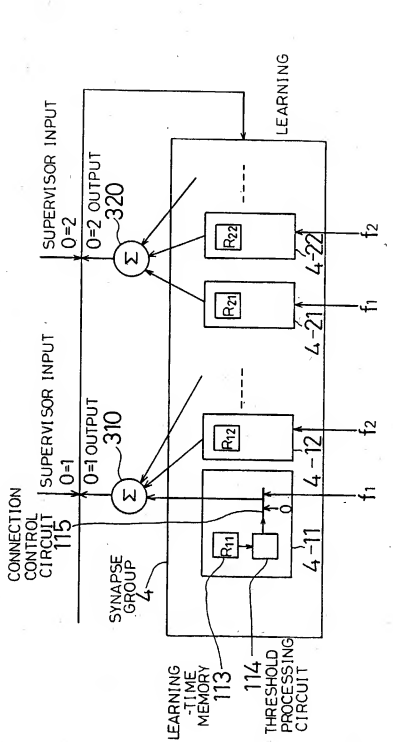
CONNECTION CONTROL CIRCUIT 115
SUPERVISOR INPUT 0=1
0=1 OUTPUT 310
SUPERVISOR INPUT 0=2
0=2 OUTPUT 320
SYNAPSE GROUP 4
LEARNING
LEARNING TIME MEMORY 113
114 THRESHOLD PROCESSING CIRCUIT
R11
R12
R21
R22
4-11
4-12
4-21
4-22
f1
f2
0

Fig.2

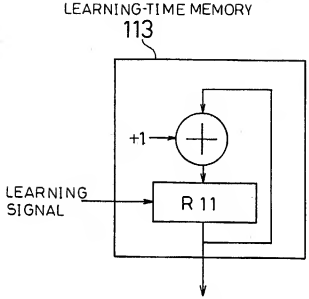
LEARNING-TIME MEMORY
113
+1
LEARNING
SIGNAL
R 11

Fig.3

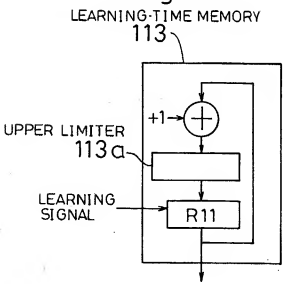
LEARNING-TIME MEMORY
113
+1
UPPER LIMITER
113a
LEARNING
SIGNAL
R11

Fig. 4

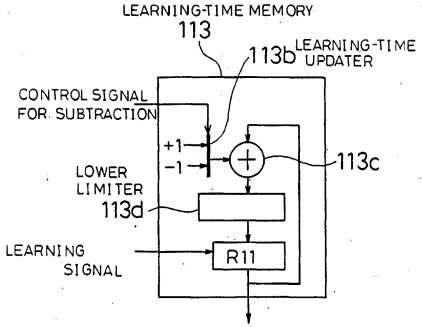
LEARNING-TIME MEMORY
113
113b
LEARNING-TIME UPDATER
CONTROL SIGNAL FOR SUBTRACTION
+1
−1
113c
LOWER LIMITER
113d
LEARNING SIGNAL
R11

Fig. 5

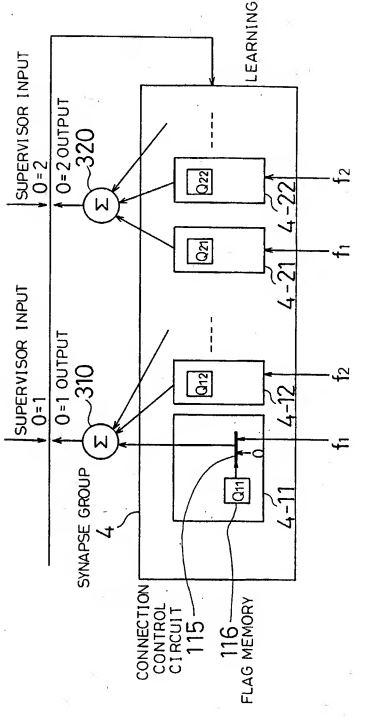
SUPERVISOR INPUT
0=1
0=1 OUTPUT
310
SUPERVISOR INPUT
0=2
0=2 OUTPUT
320
LEARNING
SYNAPSE GROUP
4
CONNECTION CONTROL CIRCUIT
115
116
FLAG MEMORY
Q11
Q12
Q21
Q22
4-11
4-12
4-21
4-22
f1
f2
f1
f2
0

Fig. 6

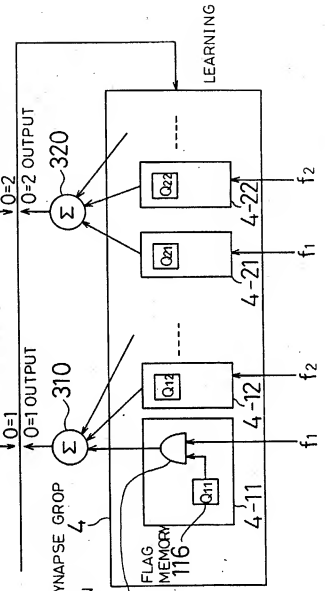
SUPERVISOR INPUT
O=1
O=1 OUTPUT
310
SUPERVISOR INPUT
O=2
O=2 OUTPUT
320
LEARNING
SYNAPSE GROP
4
CONNECTION CONTROL CIRCUIT
117
FLAG MEMORY
116
Q11
Q12
Q21
Q22
4-11
4-12
4-21
4-22
f1
f2
f1
f2

Fig.7

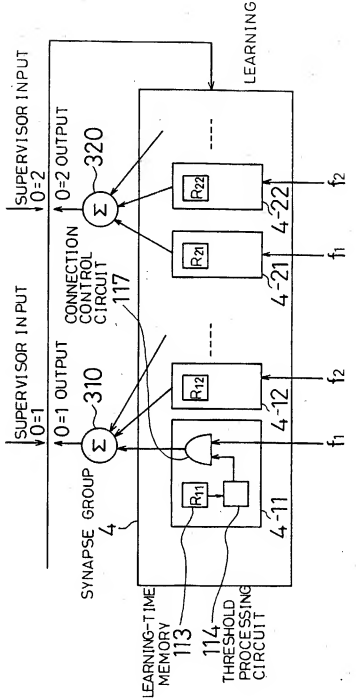
SUPERVISOR INPUT
0=1
SUPERVISOR INPUT
0=2
0=1 OUTPUT
0=2 OUTPUT
CONNECTION CONTROL CIRCUIT
117
310
320
LEARNING
SYNAPSE GROUP
4
R11
R12
R21
R22
4-11
4-12
4-21
4-22
f1
f2
f1
f2
LEARNING-TIME MEMORY
113
114
THRESHOLD PROCESSING CIRCUIT

Fig. 8

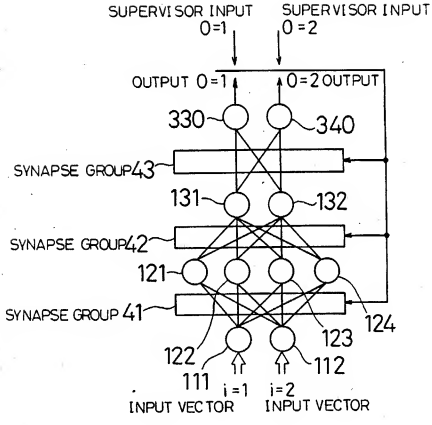
SUPERVISOR INPUT
O=1
SUPERVISOR INPUT
O=2
OUTPUT O=1
O=2 OUTPUT
330
340
SYNAPSE GROUP 43
131
132
SYNAPSE GROUP 42
121
SYNAPSE GROUP 41
124
123
122
112
111
i=1
i=2
INPUT VECTOR
INPUT VECTOR

Fig.9

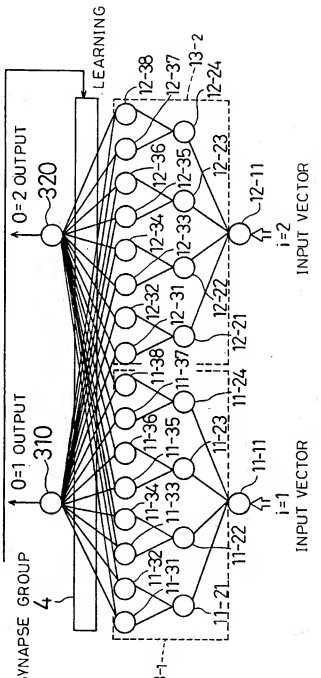
SUPERVISOR INPUT
O=1
O=1 OUTPUT
310
SYNAPSE GROUP
4
SUPERVISOR INPUT
O=2
O=2 OUTPUT
320
LEARNING
13-1
13-2
11-21
11-22
11-23
11-24
11-31
11-32
11-33
11-34
11-35
11-36
11-37
11-38
11-11
i=1
INPUT VECTOR
12-11
i=2
INPUT VECTOR
12-21
12-22
12-23
12-24
12-31
12-32
12-33
12-34
12-35
12-36
12-37
12-38

Fig.10

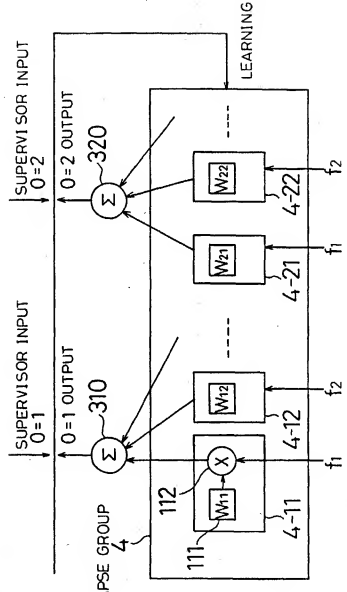
SUPERVISOR INPUT
O=1
O=1 OUTPUT
310
SUPERVISOR INPUT
O=2
O=2 OUTPUT
320
LEARNING
SYNAPSE GROUP
4
112
111
W11
W12
W21
W22
4-11
4-12
4-21
4-22
f1
f2
f1
f2

Fig.11